PCI-SIG DEVELOPERS CONFERENCE ISRAEL 2017

PCI-SIG® DEVELOPERS CONFERENCE ISRAEL 2017

September 18-19

THE HILTON TEL AVIV
Tel Aviv, Israel

AGENDA

DAY 1 - SEPTEMBER 18, 2017	
8:00 – 9:00	**Registration**
9:00 – 10:30	PCI Express® Basics & Background
10:30 – 11:00	**AM Break & Exhibit**
11:00 – 12:00	PCIe® 4.0 Electrical Update
12:00 – 1:00	**Lunch & Exhibit**
1:00 – 2:00	PCIe CEM 4.0 Previews
2:00 – 3:00	PCIe 4.0 Protocol Update
3:00 – 3:30	**PM Break & Exhibit**
3:30 – 4:30	PCIe 4.0 PHY Logical
4:30 – 5:30	PCIe Compliance Updates

DAY 2 - SEPTEMBER 19, 2017	
8:00 – 8:30	**Coffee & Exhibit**
8:30 – 9:30	Demystifying the PCIe Plug-Unplug
9:30 – 10:30	Test and Debug Challenges for PCIe 4.0
10:30 – 11:00	**AM Break & Exhibit**
11:00 – 12:00	Analysis and Validation Methodologies of Speed Transition Test Cases
12:00 – 1:00	**Lunch & Exhibit**
1:00 – 2:00	Lessons Learned Bringing Up Early Adopter PCIe 4.0 Links
2:00 – 3:00	A Software Tool for PCIe 4.0 Lane Margining
3:00 – 3:30	**PM Break & Exhibit**
3:30 – 4:30	PCI Express Architectures for High Performance Compute and Storage Systems
4:30 – 5:30	PCIe Differential Vias Design to Reduce Inter-Differential Pair Crosstalk

SPEAKERS

JOE ALLEN

Joe Allen is a Server/Storage Segment Lead at Tektronix, and is responsible for Solution Planning for PCIe, SAS, and SATA solutions. Joe has 20 years of experience in the field of high speed serial data communications, Joe holds a Bachelor's Degree in Electrical Engineering from the University of Michigan, and has completed graduate-level engineering courses at Stanford University. Prior to Tektronix, Joe has worked as an Optical Transceiver Design Engineer at IBM and Product Line Manager at JDSU and Semtech. Joe has participated in the following industry standards bodies: Optical Internetworking Forum (OIF), PCI-SIG, SASPHY/T10, and SATA IO.

JOE COWAN

Joe Cowan is a Senior Systems Architect in Hewlett Packard Enterprise. He represents HPE in the PCIe Protocol Workgroup, where he's authored numerous ECNs and errata. During his 38-year career with HP/HPE, Joe has worked in many other areas, including InfiniBand, PCI-X, chipset design, platform architecture, OS development, and security.

PELLE FORNBERG

Pelle Fornberg is a Senior Staff Engineer at Intel Corporation. He joined Intel in 2002 after receiving B.S. and M.S. degrees in Electrical Engineering from the University of Colorado at Boulder. He was involved with developing EV methodologies for high speed differential interfaces including PCI Express and Intel® QuickPath Interconnect. Pelle has spent the past 10 years within a client electrical development team where he has primarily focused on developing customer post-silicon validation tools and methodologies. Outside of the office he enjoys spending time with his wife and taking part in various outdoor activities such as sailing, camping, snowboarding and mountain biking.

DAN FROELICH

Dan Froelich is a staff engineer/ architect at Intel Corporation. He received a BS in Physics from Harvey Mudd College in 1996. Dan played key roles in the technical planning and compliance method and tool development for the USB 2.0, PCIe 1.1 and 2.0, Wireless USB and WiMedia compliance programs. He also authored portions of the PCIe 2.0 CEM, Wireless USB, USB 3.0, and WiMedia technical specifications. Dan currently chairs the PCI-SIG CEM Group and co-chairs the PCI-SIG Electrical Workgroup in addition to the Serial Enabling Group which is working on the PCI Express 4.0 Compliance Program.

VINOD HUDDAR

Vinod Arjun Huddar (Vinod A H) is currently working as a Senior Signal Integrity & Power Integrity Engineer for Seagate HDD India. He graduated in 2007 from University Visvesvaraya College of Engineering (U.V.C.E) in Bangalore, Karnataka, India as an Electronics & Communication Engineer. His past experience is with Nvidia Corporation & Echostar Corporation with 10 years of experience in Signal Integrity & Power Integrity.

ISAAC LIVNY

Isaac Livny has been following PCI Express technology since its incubation taking over PCI and PCI-X. Isaac has been involved in the design and system integration of a variety of PCI Express products during his 16 years of employment in LSI. The past 7 years in the Protocol Systems Group of Teledyne Lecroy, Isaac has been covering the applications of protocol analysis and traffic generation of a large variety of technologies, focusing on architectural aspects, compliance and validation of PCIe and specifically NVMe devices. Isaac's contribution played a notable role bringing the Teledyne Lecroy NVMe analysis and traffic generation tools to the leading position they reached in the industry.

DEREK PERCIVAL

Derek Percival is a Senior FAE for Broadcom Ltd covering EMEA for Broadcom's range of PCIe switches and bridges. He has been providing technical support and educational seminars on PCI and PCIe based products for the last seventeen years. Derek holds a BSc EE and a Diploma in Engineering from Hull University, UK.

RICHARD SOLOMON

Richard Solomon is the Technical Marketing Manager for Synopsys' DesignWare PCI Express Controller IP. He has been involved in the development of PCI chips dating back to the NCR 53C810 and pre-1.0 versions of the PCI spec. Richard architected and led the development of the PCI Express and PCI-X interface cores used in an industry-leading line of storage RAID controller chips. He has served on the PCI-SIG Board of Directors for over 10 years, and continues to represent Synopsys on wide variety of PCI workgroups. Richard holds a B.S.E.E. from Rice University and 26 US Patents, many of which relate to PCI technology.

ALEX UMANSKY

Alex Umansky is a Chief Architect at Huawei, IT Product Line, where he defines PCI Express solutions for Servers, Cloud and Storage platforms. He has close to 16 years of experience in developing PCI Express silicones and systems starting PCIe IP cores in IBM design labs based on first drafts of 3GIO (later renamed to PCI Express) spec. During his career Alex has worked in many areas, including InfiniBand, PCIe IPs/Switches, advanced IO virtualization solutions, NextGen switch fabrics and programmable engines for networking packet processing and traffic management.

PRESENTATION ABSTRACTS

DAY 1 – PCI-SIG® TECHNOLOGY SEMINAR

PCI Express® Basics & Background

Presenter: Richard Solomon

In this session, attendees will learn the basics of the PCI Express Architecture. This presentation will cover the key features of PCI Express and provide an overview of the Electrical, Packet-Based Protocol and Configuration Mechanism of this high performance serial bus architecture. This session is geared towards attendees new to PCI Express technologies.

PCIe 4.0 Electrical Update

Presenter: Dan Froelich

In transitioning to PCIe 4.0 the raw data rate is being doubled to 16GT/s keeping the same efficient encoding used for the PCIe 3.0 8GT/s data rate. The PCIe 4.0 Base Specification divides up the electrical layer into four components: Transmitter, Channel, Receiver and Reference Clock. The PCIe 4.0 preliminary specification for each component will be discussed along with the rationale behind the parameters specified and the measurement methodologies and potential updates to methodologies under discussion for PCIe 4.0. This session is geared toward experienced PCI Express PHY designers and validation engineers.

PCIe CEM 4.0 Previews

Presenter: Dan Froelich

This presentation provides updates on the recent PCI Express specification development work in the PCI-SIG Electromechanical Workgroup. The presentation focuses on providing an overview of the preliminary PCI Express Card Electromechanical Specification 4.0 (CEM 4.0) and provides an overview of several potential improvements under investigation to improve the CEM connector to support 16GT/s signaling while maintaining backwards compatibility.

PCIe 4.0 Protocol Update

Presenter: Joe Cowan

This session covers PCI Express protocol changes over the last two years or so, including completed ECNs, selected ECRs under development, and major changes developed for PCIe 4.0. Completed ECNs include Emergency Power Reduction with PWRBRK Signal, RC Integrated Endpoint & IOV Updates, Expanded Resizable BARs, Extended Message Data for MSI, SR-IOV Table Updates, VF Resizable BARs, Flattening Portal Bridge (FPB), and Hierarchy ID Message. Selected ECRs under development include Firmware Validation and Native PCIe Enclosure Management (NPEM). Major PCIe 4.0 protocol changes involve 10-Bit Tags, Scaled Flow Control, simplified protocol timers, and the incorporation of other PCI specifications into the PCIe Base specification.

PCIe 4.0 PHY Logical

Presenter: Joe Cowan

This session will cover important aspects of the PCIe 4.0 Logical PHY specification as it is being developed. The talk will focus on the PCIe 4.0 encoding, Tx equalization, enhancements to the per-Lane error logging mechanism to work with retimers, Ordered Set changes to meet the PCIe 4.0 Data Rate, compliance pattern, and Lane Margining at Receiver. People who are designing, validating, or specifying the latest generation of PCIe components are the target audience for this session.

PCIe Compliance Updates

Presenter: Richard Solomon

This presentation outlines the requirements for PCI Express compliance and interoperability. It provides an overview of all testing performed for the PCIe 3.x and PCIe 2.x compliance programs—with a focus on updates/changes for the 3.x program and first look at PCIe 4.0. Every component of the PCIe compliance program is discussed including electrical, protocol, platform BIOS, and configuration testing. This session will also cover the timeline for upcoming Compliance Workshop events worldwide, where members can validate their parts for compliance to the PCI-SIG "Gold" suite of tests.

DAY 2 – MEMBERS IMPLEMENTATION

Demystifying the PCIe Plug-Unplug

Presenter: Alex Umansky

The Hot Plug and Unplug of PCIe devices has always presented a major challenge for silicon, systems and software developers. The rapidly growing popularity of PCIe SSDs in Data Centers gives rise to the need for effective solutions allowing surprising disconnect of devices, without system crashes and performance degradation. The presentation explores several plug and unplug hardware detection methods including the procedures described in the specification and also some best practices that de-facto became industry "standards". Plug-unplug software techniques are described along with discussions on timing and resources allocation restrictions. Recent changes to the specification and related configuration capabilities are covered. And finally, the presentation is a call for further discussions by the committee members.

Test and Debug Challenges for PCIe 4.0

Presenter: Joe Allen

As design margins shrink, accurate and standard-specific measurement is key to debugging, verifying design and performing interoperability testing when designing PCIe devices. Having confidence in test processes, workflows and results will allow you to reach compliance faster. This presentation will provide the information you need to do just that. We will discuss the most recent PCIe standards requirements and provide an in-depth look at: PCIe Transmitter (Tx) and Receiver (Rx) Compliance Testing, Current Testing Challenges and Solutions for both Tx and Rx PCIe 1.0-4.0, including PHY and protocol-aware testing, Debugging Loopback Initiation and Link Training with protocol-aware BERTScope and high-bandwidth oscilloscope, and look to challenges and solutions for PCIe 5.0.

Analysis and Validation Methodologies of Speed Transition Test Cases

Presenter: Isaac Livny

As PCIe specifications are climbing up the speed ladder, validating and analyzing speed transition challenges increase. While 2.5 and 5 gig speeds use fixed de-emphasis, 8 and 16 gig speeds require Tx/Rx equalization. While 5 and 8 gig speeds are negotiated to the highest advertised speed, transition to 16 gig is stepping through an 8 gig equalizer. This presentation will cover analysis methods of link training and dynamic equalization as well as traffic generation techniques used to validate speed transition specifications. We discuss failure examples covered by PCI-SIG compliance such as reject and phase transition time limits, and incompliant behaviors that require additional validation tests. We conclude by showing how to incorporate a sequence of validation tests into a test automation environment.

Lessons Learned Bringing Up Early Adopter PCIe 4.0 Links

Presenter: Richard Solomon

This presentation covers pitfalls found trying to interoperate early adopter designs supporting 0.5 and 0.7 drafts of the PCIe 4.0 specification. Initial link bringups are always challenging, and mixing pre-release devices adds further complexity. The presentation will show design for debug features that can be incorporated to assist, as well as methods for using standard test tools and PCIe-specific knowledge to determine WHY a link is not coming up, not staying up, or not negotiating the desired speed. These tools and techniques will also provide valuable insight for first adopters who will be integrating final PCIe 4.0 devices upon release.

A Software Tool for PCIe 4.0 Lane Margining

Presenter: Pelle Fornberg

The PCI Express 4.0 Specification introduces an Rx lane margining requirement for all endpoints, root ports and retimers. This presentation will provide details on the development of a software tool that is being developed to enable the margining of PCI Express 4.0 devices. The tool and associated reference code is intended to be delivered by the PCI-SIG to its members. The purpose of this presentation is to educate the PCI-SIG community on the effort that is underway on the development of this tool, communicate the present development status and to provide details on features and capabilities it will provide.

PCI Express Architectures for High Performance Compute and Storage Systems

Presenter: Derek Percival

With its high bandwidth and low latency PCI Express is ideally suited to high performance compute and storage systems. This presentation outlines how PCI Express is being used in more complex architectures to create rack scale resource pooling of compute and storage systems, artificial intelligence and hyperscale systems. The presentation will also cover how data can be moved between compute nodes without going through latency and loss prone external Routers or Switches. Additional topics such as how resources can be moved and/or shared between compute nodes within rack scale systems will also be discussed.

PCIe Differential Vias Design to Reduce Inter-Differential Pair Crosstalk

Presenter: Vinod A H

PCIe traces spread apart before entering differential via. This causes differential impedance to increase at via. If the stack-up is 4 layers & impedance of differential trace is 85 Ohms like in the case of the PCIe interface, having lesser layers results in lesser capacitive effect and spreading the traces will make the impedance to go higher. There are many via designs which can address issues like adding ground via in between etc. It is usual to have multiple differential pairs like PCIe x16 or x32 interface where 16 or 32 differential pairs are routed together. Via crosstalk is an issue as multiple differential vias come in parallel to each other. Crosstalk control can be done using traditional approaches like spacing via pair far apart. We propose a PCIe via structure to solve the crosstalk problem with reduced PCB real estate, without modifying single ended 50 Ohms impedance & differential 85 Ohms impedance.

SPONSORS

Keysight Technologies

Keysight Technologies is a leading technology company that helps its engineering, enterprise and service provider customers optimize networks and bring electronic products to market faster and at a lower cost. No matter the generation of PCI Express design being tested, Keysight offers a complete solution set from design simulation, to prototype validation, to manufacturing and compliance testing. Work with Keysight and gain insights into your best PCIe design. **www.keysight.com**

Mentor®, A Siemens Business

Mentor®, A Siemens Business, offers a comprehensive PCI Express® verification IP solution that includes SystemVerilog UVM Verification IP (VIP) for fastest time to verification sign-off, and seamless integration into both simulation and emulation environments.

Synopsys

It is a competitive market, finish first with Synopsys' silicon-proven DesignWare® IP solutions for PCI Express® – controllers, PHYs, verification IP, IP Prototyping Kits, Software Development Kits and Interface IP Subsystems. The IP is designed to the latest PCI Express and PIPE specifications, has gone through extensive interoperability testing and is shipping in volume production, enabling designers to accelerate time-to-market and reduce integration risk. **www.synopsys.com/pcie.**

Tektronix

Tektronix is renowned as a leading manufacturer of test solutions who specializes in automated measurement suites that speed up PHY validation cycles and ensure consistency of majority of High Speed Serial technologies such as PCIe, Thunderbolt, HDMI, SATA/SAS, USB, MHL, DP, MiPi etc. Visit our booth to learn how we can help you accelerate the analysis, validation, and precompliance or perform device characterization or protocol debug testing of your PCIe designs with test solutions from Tektronix.

Teledyne LeCroy

Teledyne LeCroy is a worldwide leader in serial data test solutions, creating advanced instruments that drive product innovation by quickly measuring, analyzing, and verifying complex electronic signals. The company offers high-performance oscilloscopes, serial data analyzers, and protocol test solutions. These products' features include wave form analysis at the PCI Express physical layer, analyzing at the protocol level from the packet to the command layer and testing compliance at the physical, link and transaction layers.
http://www.teledynelecroy.com

Viavi Solutions

Viavi is a new global company created from the people, expertise and technology of JDSU's successful test and measurement and network and service enablement offerings. Come by our booth to see features of our PCIe and NVMe storage protocol Analyzers, Jammers, and an assortment of probes including M.2, SFF-8639, and SFF-8644.

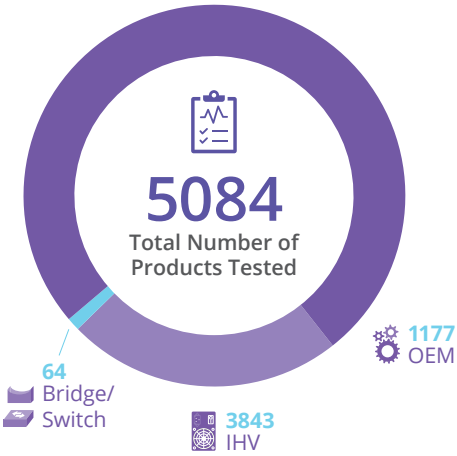
HISTORY OF PCI-SIG®

CELEBRATING 25 YEARS 1992 2017 PCI-SIG OF INNOVATION

3600
Total Number of Companies Involved

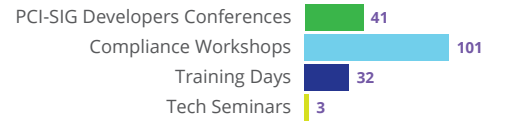
CURRENT
730+ member companies located worldwide

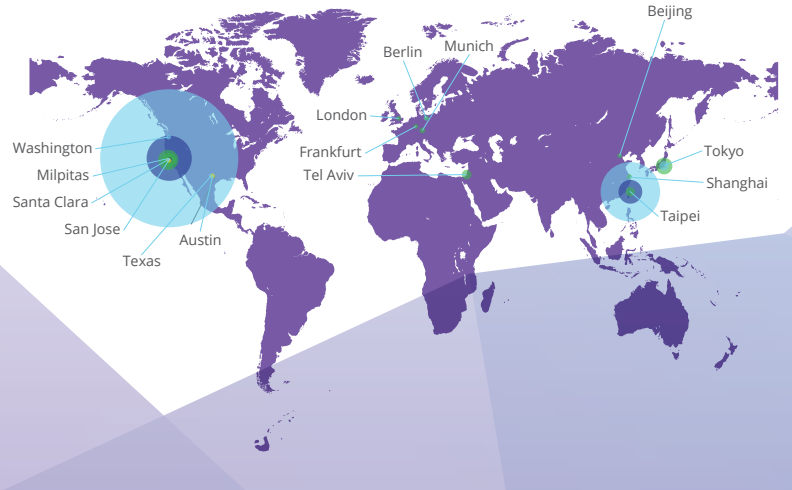
40%
Percentage of enterprise SSD revenue expected from PCIe-based SSD sales by 2019



Where in the world is PCI-SIG?

177
Total Events

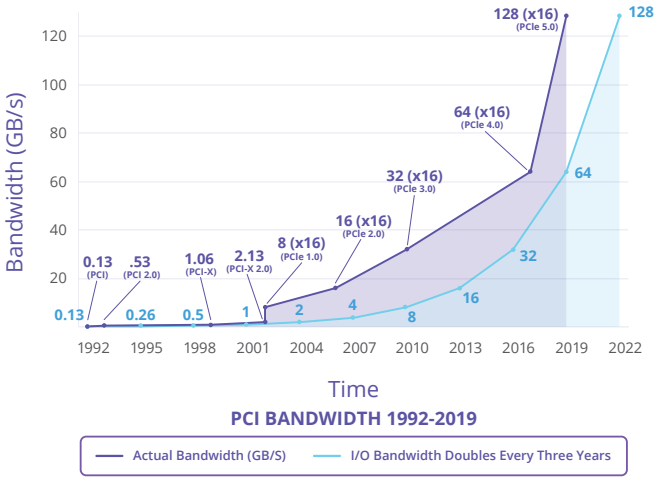




PCI-SIG History

I/O BANDWIDTH DOUBLES

Every 3 Years



30 Major Specifications Published

PCI EXPRESS®

- PCI Express Base Specification
- PCI Express Card Electromechanical Specification
- PCI Express M.2 Specification
- PCI Code and ID Assignment Specification
- PCI Express Connector High Speed Electrical
- PCI Express OCuLink Specification
- PCI Express Architecture Mobile Graphics Lo-Power Addendum to the PCI Express Base Specification
- Multi-Root I/O Virtualization and Sharing Specification
- Single Root I/O Virtualization and Sharing Specification
- Address Translation Services
- PCI Express External Cabling Specification
- PCI Express ExpressModule Electromechanical Specification
- PCI Express x16 Graphics 150W-ATX Specification
- PCI Express to PCI/PCI-X Bridge Specification
- PCI Express Mini Card Electromechanical Specification
- PCI Express 225 W/300 W High Power Card Electromechanical

CONVENTIONAL PCI

- PCI Local Bus
- PCI Firmware Specification
- Mini PCI Specification 1.0
- PCI Bios Specification Revision 2.1
- PCI Standard Hot-Plug Controller and Subsystem Specification
- PCI Hot-Plug Specification
- PCI-to-PCI Bridge Architecture Specification

PCI-X

- PCI-X 2.0 Electrical Report
- PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification
- PCI-X Protocol Addendum to the PCI Local Bus Specification

PCI EXPRESS® - TEST SPECIFICATIONS

- PCI Express Architecture Platform Init / Config
- PCI Express Architecture Link Layer and Transaction Layer
- PCI Express Architecture Configuration Space
- PCI Express Architecture PHY

PCI-SIG Developers Conference Israel 2017

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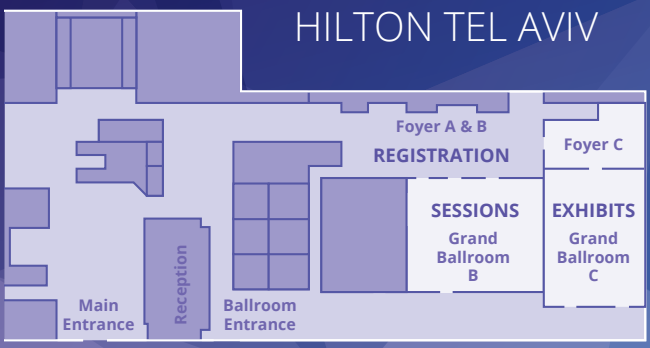
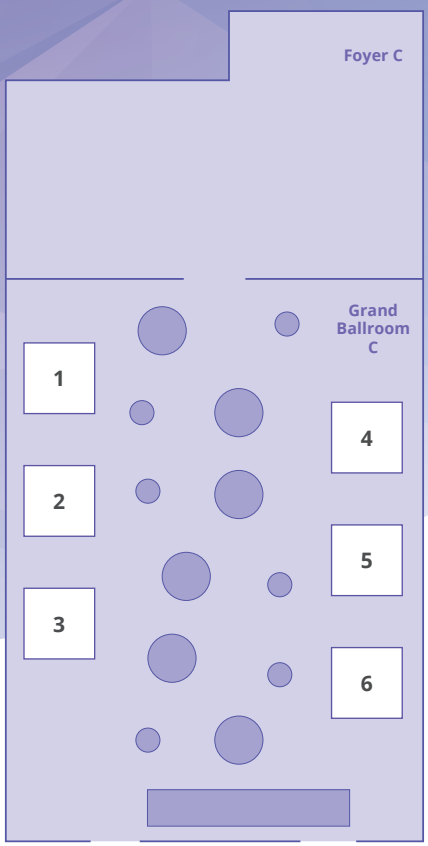


EXHIBIT AREA



Company	Booth #
Keysight Technologies	3
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Synopsys	1
Tektronix	6
Teledyne LeCroy	5
Viavi Solutions	2

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